Application No.: 10/612,945 Docket No.: 8733.330.10-US

## AMENDMENTS TO THE CLAIMS

## 1-15. (Canceled)

16. (Currently Amended): A method of fabricating a thin film transistor, comprising: providing a substrate;

depositing amorphous silicon on the substrate;

patterning the amorphous silicon to form <u>a plurality of [[plural]]</u> island-shaped amorphous silicon layers;

forming spaces between the substrate and the amorphous silicon layers;

forming a channel region, a source <u>ohmic contact</u> region, and <u>a</u> drain ohmic contact region [[regions]] on each of the amorphous silicon layers by ion doping the island-shaped amorphous silicon layers;

forming a first insulating layer over the amorphous silicon layers;

crystallizing the plurality of the island-shaped amorphous silicon layers the amorphous silicon layers to form a plurality of an island-shaped polysilicon layers by irradiating laser beams onto the first insulating layer, wherein the plurality of the island-shaped polysilicon layers are the active layers of the thin film transistor;

forming a gate electrode on the first insulating layer; and

forming source and drain electrodes that contact the source and drain ohmic contact regions, respectively.

- 17. (Currently Amended): The method of claim 16, wherein the forming of the channel region, the source ohmic contact region, and the drain ohmic contact region [[regions]] on each of the amorphous silicon layers is performed by forming ion stoppers on the island-shaped amorphous silicon layers, using the ion stoppers as masks during doping, and then removing the ion stoppers.
- 18. (Original): The method of claim 16, wherein the spaces are formed by etching an upper side of the substrate.

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19. (Original): The method of claim 16, wherein the spaces are formed by depositing a space-forming layer between the substrate and the amorphous silicon, and then patterning the space-forming layer to form the spaces therein.

- 20. (Original): The method of claim 16, wherein the source and drain electrodes are formed under the active layers.
- 21. (Original): The method of claim 16, further including forming a second insulating layer on the gate electrode such that the second insulating layer includes contact holes that expose the source and drain ohmic contact regions.
- 22. (Original): The method of claim 21, further including forming source and drain electrodes on the second insulating layers that contact the active layers via the contact holes.
- 23. (Currently Amended): The method of claim 20, further including forming doped the source and drain ohmic contact regions having island-shapes on the source and drain electrodes.
- 24. (Original): The method of claim 23, wherein the source and drain regions are formed of amorphous silicon.
- 25. (Original): The method of claim 23, wherein the source and drain regions are formed in contact with the plurality of active layers.

26-29. (Canceled)